IN THE CLAIMS:

This listing of claims will replace all prior versions, and listings, of claims in the application.

1. (Previously Presented) A semiconductor device comprising a memory thin film transistor comprising:

an insulating surface;

an active layer over the insulating surface, comprising a source region, a drain region and a channel forming region;

a first insulating film formed on the active layer;

a floating gate formed on the first insulating film;

a second insulating film formed on the floating gate;

a control gate formed on the second insulating film; and

a first region and a second region included in the channel forming region,

wherein a thickness of the first insulating film on the second region is thinner than a thickness of the first insulating film on the first region,

wherein a concentration of impurity elements in the first region is larger than a concentration of impurity elements in the second region, and

wherein the impurity elements are any one of P-type impurity elements and N-type impurity elements.

2.-3. (Canceled)

4. (Original) A semiconductor device according to claim 1, wherein the memory transistor stores multi-value information.

5. (Canceled)

6. (Original) A semiconductor device according to claim 1, wherein the semiconductor device is an electronic device selected from the group consisting of a video camera, a digital camera, a head-mount type of display, a DVD player, a game machine, a goggle type of display, a car navigation apparatus, an acoustic playback apparatus, a personal computer and a portable information terminal.

7. (Currently Amended) A semiconductor device comprising a memory transistor comprising:

an insulating surface;

an active layer over the insulating surface, comprising a source region, a drain region and a channel forming region;

~~a first region and a second region formed in the channel forming region;~~

a first insulating film formed on the active layer;

a floating gate formed on the first insulating film;

a second insulating film formed on the floating gate;

a control gate comprising metal thin film formed on the second insulating film; and

a first region and a second region included in the channel forming region,

wherein a concentration of impurity elements in the first region is larger than a concentration of impurity elements in the second region, and

wherein the impurity elements are any one of P-type impurity elements and N-type impurity elements.

8.-9. (Canceled)

10. (Original) A semiconductor device according to claim 7, wherein the memory transistor stores multi-value information.

11. (Original) A semiconductor device according to claim 7, wherein the memory transistor is formed on a substrate selected from the group consisting of a single crystal semiconductor substrate, a substrate having an insulating surface and a SOI substrate.

12. (Original) A semiconductor device according to claim 7, wherein the semiconductor device is an electronic device selected from the group consisting of a video camera, a digital camera, a head-mount type of display, a DVD player, a game machine, a goggle type of display, a car navigation apparatus, an acoustic playback apparatus, a personal computer and a portable information terminal.

13. (Currently Amended) A semiconductor device comprising a memory cell comprising:

an active layer comprising a first channel forming region interposed between a source region and a source/drain region, and a second channel forming region interposed between the source/drain region and a drain region;

a first insulating film formed on the active layer;

a first floating gate and a second floating gate formed on the first insulating film;

a second insulating film formed on the first floating gate and the second floating gate; and

a first control gate and a second control gate formed on the second insulating film,

wherein a thickness of the first insulating film on the second channel forming region is thinner than a thickness of the first insulating film on the first channel forming region,

wherein the first floating gate and second floating gate are connected to each other, and

wherein the first control gate and second control gate are connected to each other, and

wherein ~~each concentration~~ concentrations of the impurity elements of the source region, the source/drain region and the drain region ~~is~~ are formed to be the same ~~intentionally~~.

14.-15. (Canceled)

16. (Previously Presented) A semiconductor device according to claim 13, wherein the memory cell stores multi-value information.

17. (Previously Presented) The semiconductor device according to claim 13, wherein the memory cell is formed on a substrate selected from the group consisting of a single crystal semiconductor substrate, a substrate having an insulating surface and a SOI substrate.

18. (Original) A semiconductor device according to claim 13, wherein the semiconductor device is an electronic device selected from the group consisting of a video camera, a digital camera, a head-mount type of display, a DVD player, a game machine, a goggle type of display, a car navigation apparatus, an acoustic playback apparatus, a personal computer and a portable information terminal.

19. (Original) A semiconductor device according to claim 13, wherein a threshold voltage of the first channel forming region is different from a threshold voltage of the second channel forming region.

20. (Canceled)

21. (Currently Amended) A semiconductor device comprising a memory cell comprising:

an active layer comprising a first channel forming region interposed between a source region and a source/drain region, and a second channel forming region interposed between the source/drain region and a drain region;

a first insulating film formed on the active layer;

a first floating gate and a second floating gate formed on the first insulating film;

a second insulating film formed on the first floating gate and second floating gate; and

a first control gate and a second control gate formed on the second insulating film,

wherein a concentration of impurity elements in the first region is larger than a concentration of impurity elements in the second region,

wherein the impurity elements are any one of P-type impurity elements and N-type impurity elements,

wherein the first floating gate and second floating gate are connected to each other, and

wherein the first control gate and second control gate are connected to each other, and

wherein ~~each concentration~~ concentrations of the impurity elements of the source region, the source/drain region and the drain region ~~is~~ are formed to be the same ~~intentionally~~.

22.-23. (Canceled)

24. (Previously Presented) A semiconductor device according to claim 21, wherein the memory cell stores multi-value information.

25. (Previously Presented) A semiconductor device according to claim 21, wherein the memory cell are formed on a substrate selected from the group consisting of a single crystal semiconductor substrate, a substrate having an insulating surface and a SOI substrate.

26. (Original) A semiconductor device according to claim 21, wherein the semiconductor device is an electronic device selected from the group consisting of a video camera, a digital camera, a head-mount type of display, a DVD player, a game machine, a goggle type of display, a car navigation apparatus, an acoustic playback apparatus, a personal computer and a portable information terminal.

27. (Original) A semiconductor device according to claim 21, wherein a threshold voltage of the first channel forming region is different from a threshold voltage of threshold channel forming region.

28.-42. (Canceled)

43. (Previously Presented) A semiconductor device comprising a memory thin film transistor comprising:

an insulating substrate;

an active layer over the insulating substrate, comprising a source region, a drain region and a channel forming region;

a first insulating film formed on the active layer;

a floating gate formed on the first insulating film;

a second insulating film formed on the floating gate;

a control gate formed on the second insulating film; and

a first region and a second region included in the channel forming region,

wherein a threshold voltage of the second region is larger than a threshold voltage of the first region, and

wherein the control gate is not in contact with the first insulating film,

wherein a concentration of impurity elements in the first region is larger than a concentration of impurity elements in the second region, and

wherein the impurity elements are any one of P-type impurity elements and N-type impurity elements.

44. (Previously Presented) A semiconductor device according to claim 43, wherein the memory transistor stores multi-value information.

45. (Canceled)

46. (Previously Presented) A semiconductor device according to claim 43, wherein the semiconductor device is an electronic device selected from the group consisting of a video camera, a digital camera, a head-mount type of display, a DVD player, a game machine, a goggle

type of display, a car navigation apparatus, an acoustic playback apparatus, a personal computer and a portable information terminal.

47. (Currently Amended) A semiconductor device comprising a memory cell comprising:

an active layer comprising a first channel forming region interposed between a source region and a source/drain region, and a second channel forming region interposed between the source/drain region and a drain region;

a first insulating film formed on the active layer;

a first floating gate and a second floating gate formed on the first insulating film;

a second insulating film formed on the first floating gate and second floating gate; and

a first control gate and a second control gate formed on the second insulating film,

wherein a threshold voltage of the second region is larger than a threshold voltage of the first region,

wherein the control gate is not in contact with the first insulating film,

wherein the first floating gate and second floating gate are connected to each other, and

wherein the first control gate and second control gate are connected to each other, and

wherein ~~each concentration~~ concentrations of the impurity elements of the source region, the source/drain region and the drain region ~~is~~ are formed to be the same ~~intentionally~~.

48. (Previously Presented) A semiconductor device according to claim 47, wherein the memory transistor stores multi-value information.

49. (Previously Presented) A semiconductor device according to claim 47, wherein the memory transistor is formed on a substrate selected from the group consisting of a single crystal semiconductor substrate, a substrate having an insulating surface and a SOI substrate.

50. (Previously Presented) A semiconductor device according to claim 47, wherein the semiconductor device is an electronic device selected from the group consisting of a video camera, a digital camera, a head-mount type of display, a DVD player, a game machine, a goggle type of display, a car navigation apparatus, an acoustic playback apparatus, a personal computer and a portable information terminal.